

**FIG. 1**  
(PRIOR ART)

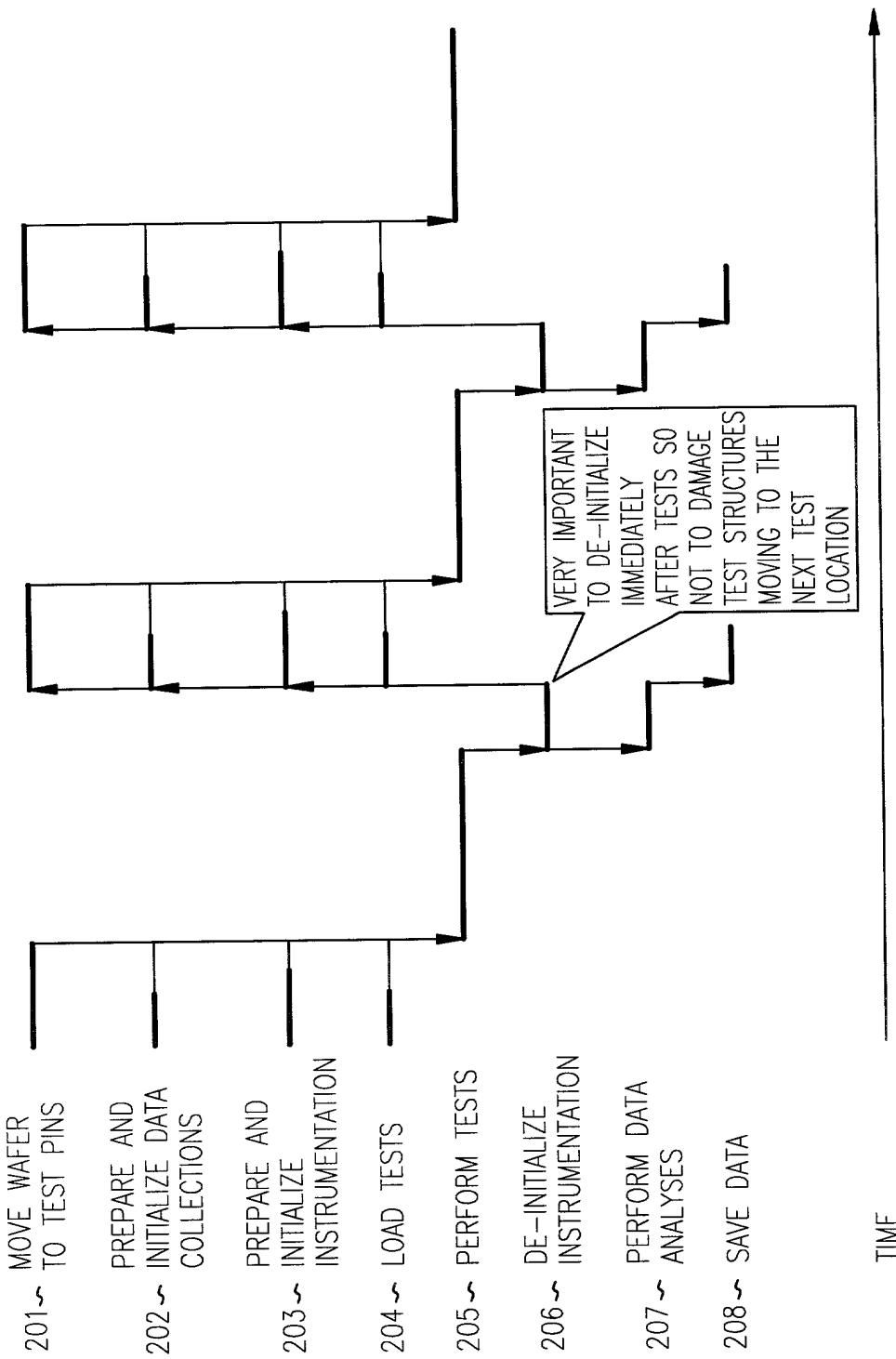


FIG. 2

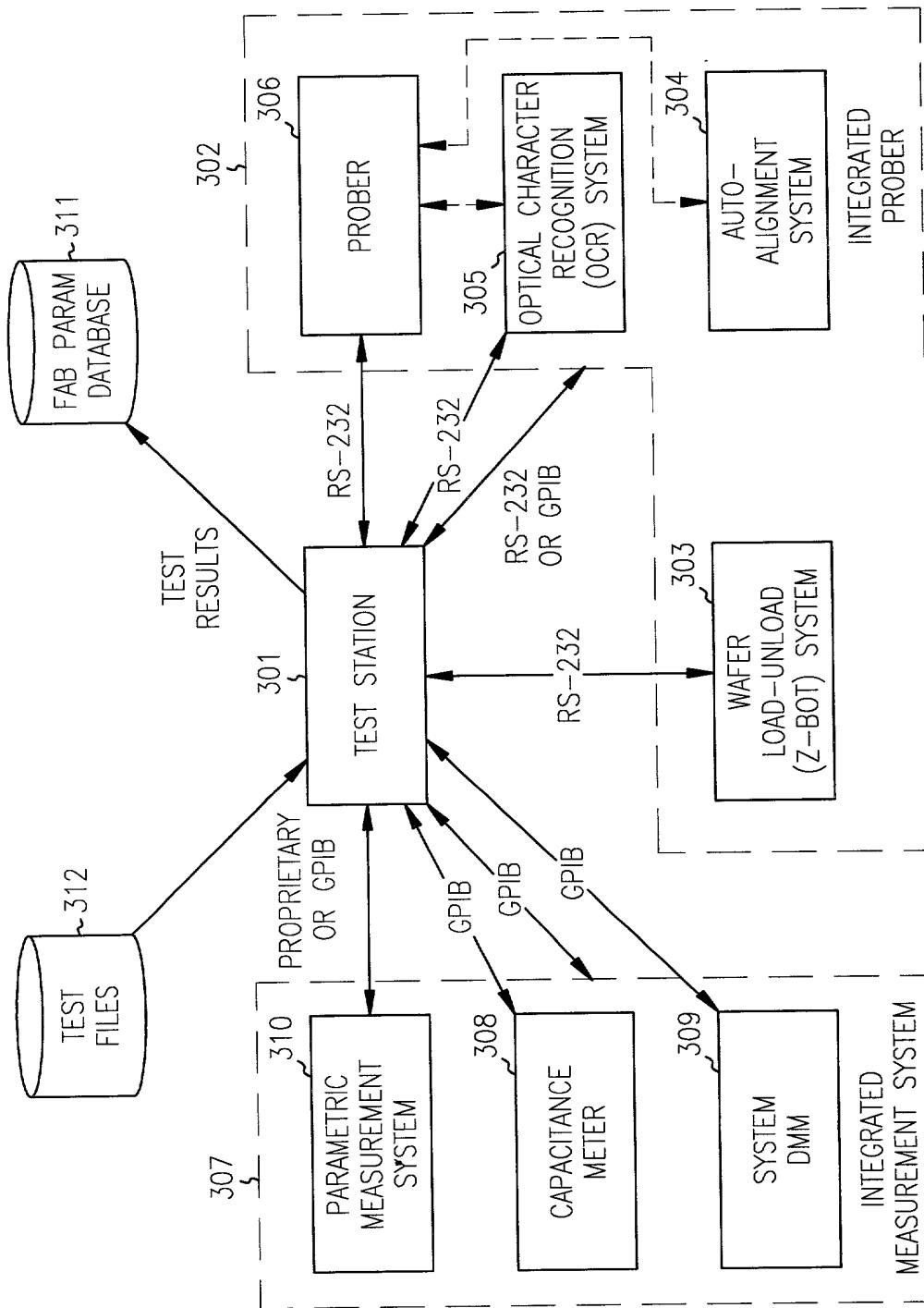
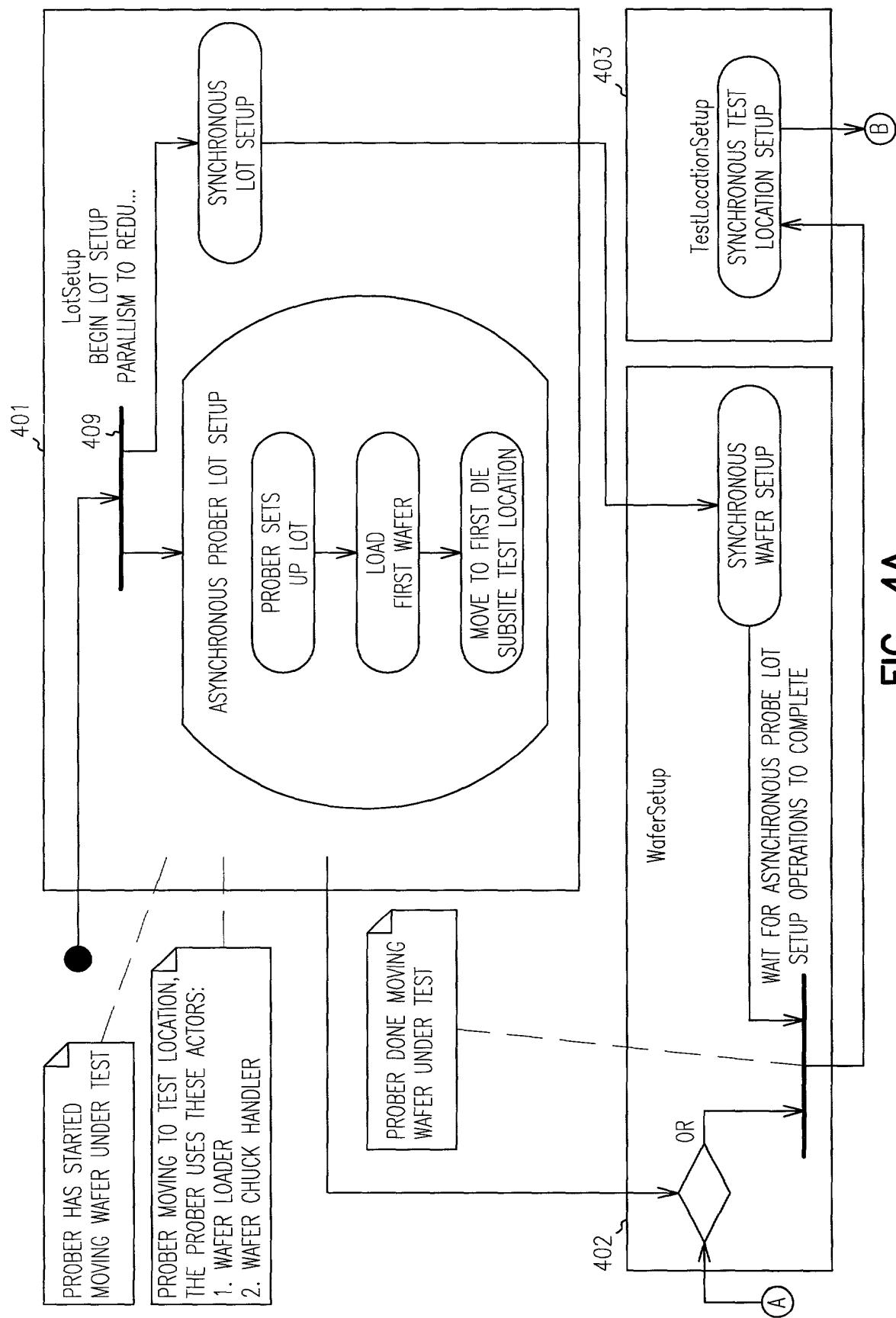


FIG. 3

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**FIG. 4A**

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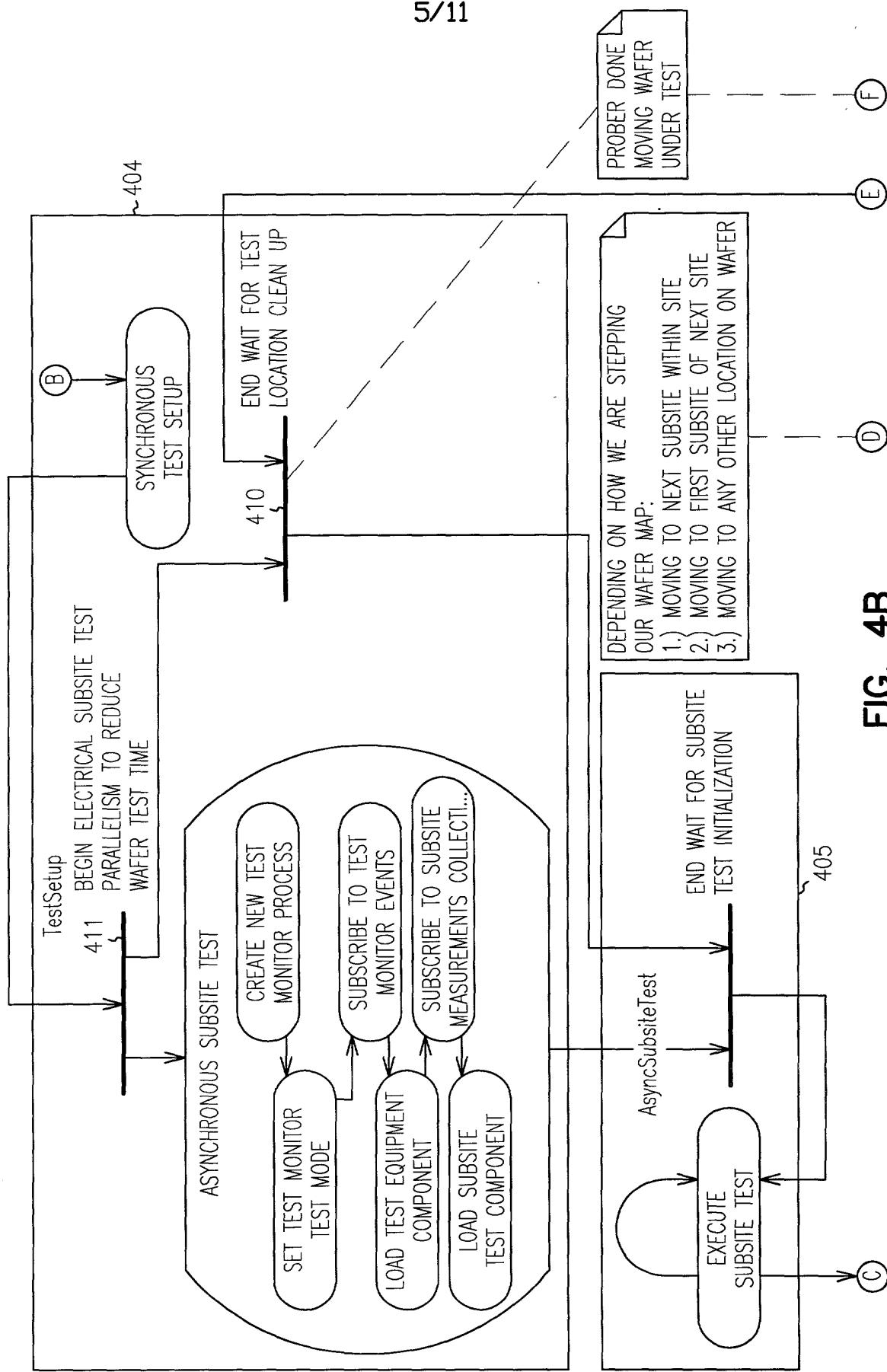


FIG. 4B

TITLE: CONCURRENT CONTROL OF SEMICONDUCTOR PARAMETRIC TESTING

INVENTORS NAME: Sergey A. Velichko et al.

SERIAL NO.: 09/834,751

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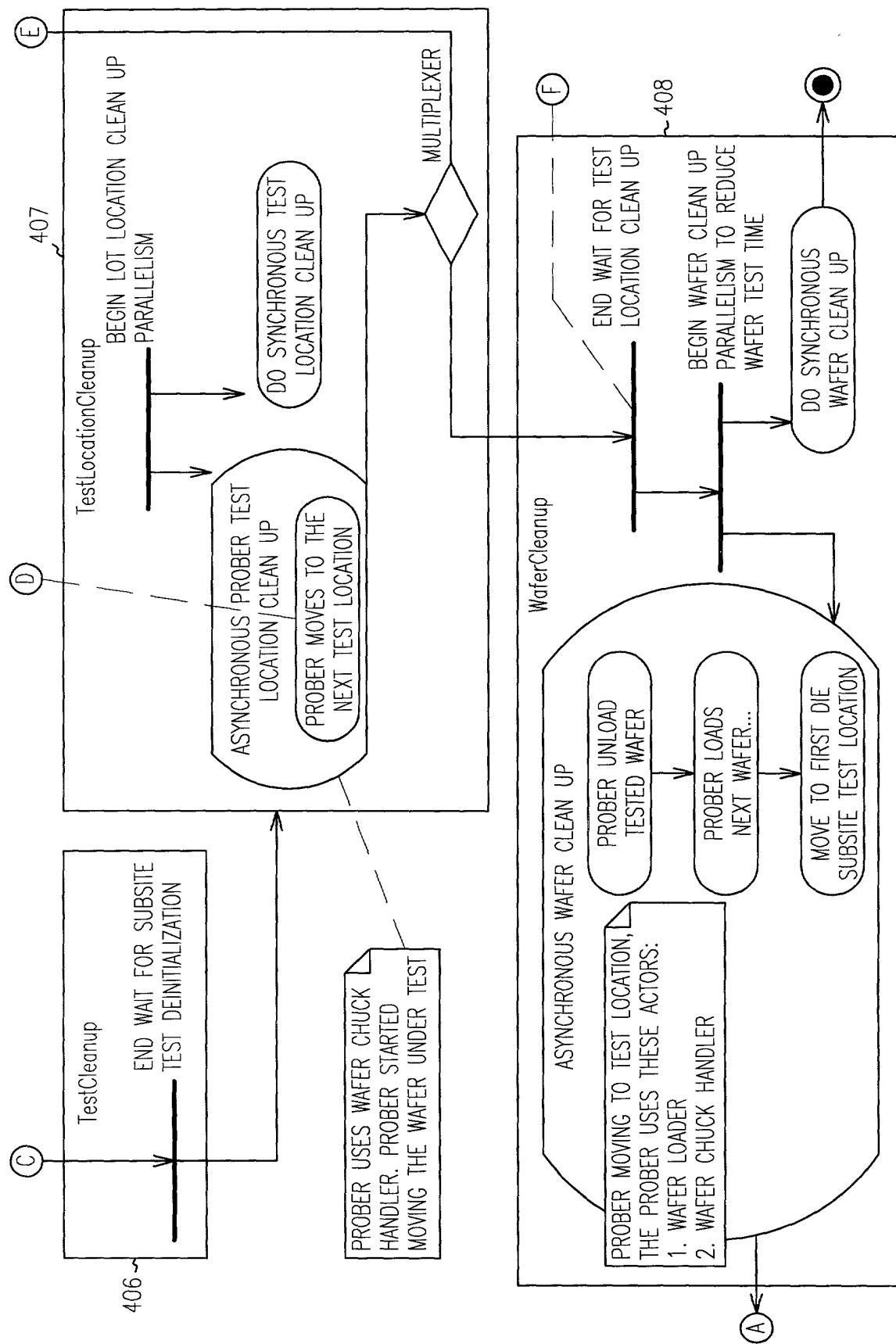


FIG. 4C

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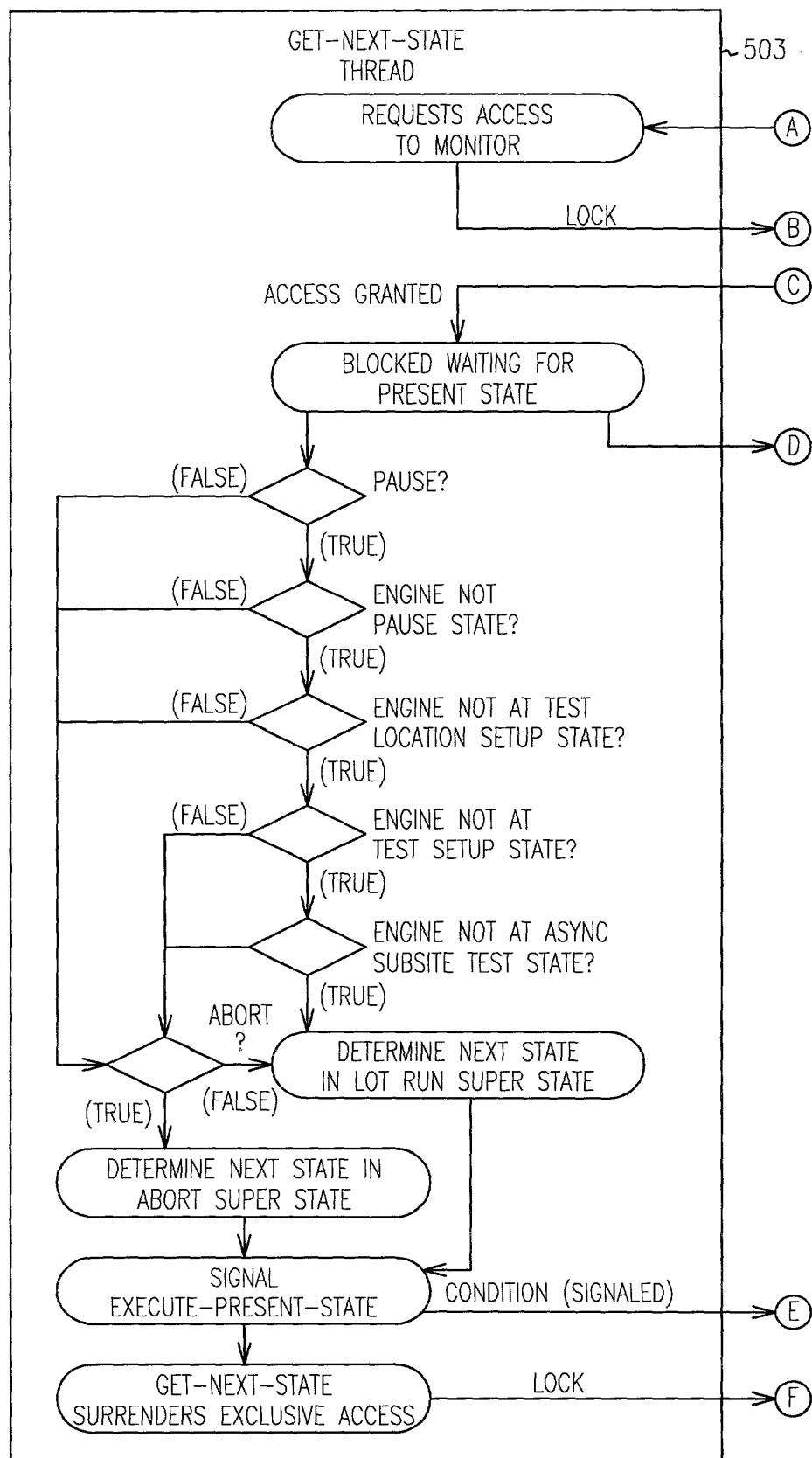


FIG. 5A

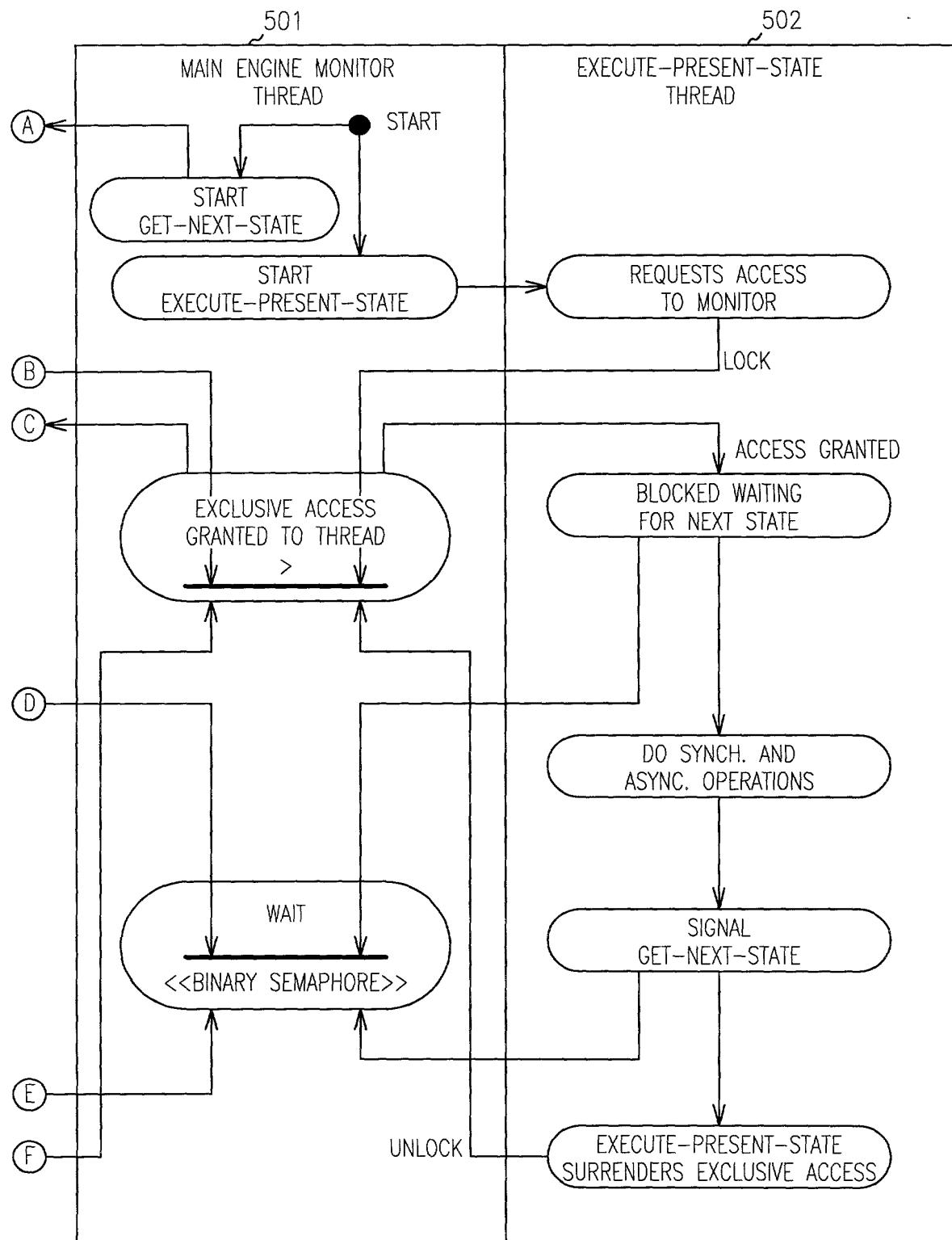


FIG. 5B

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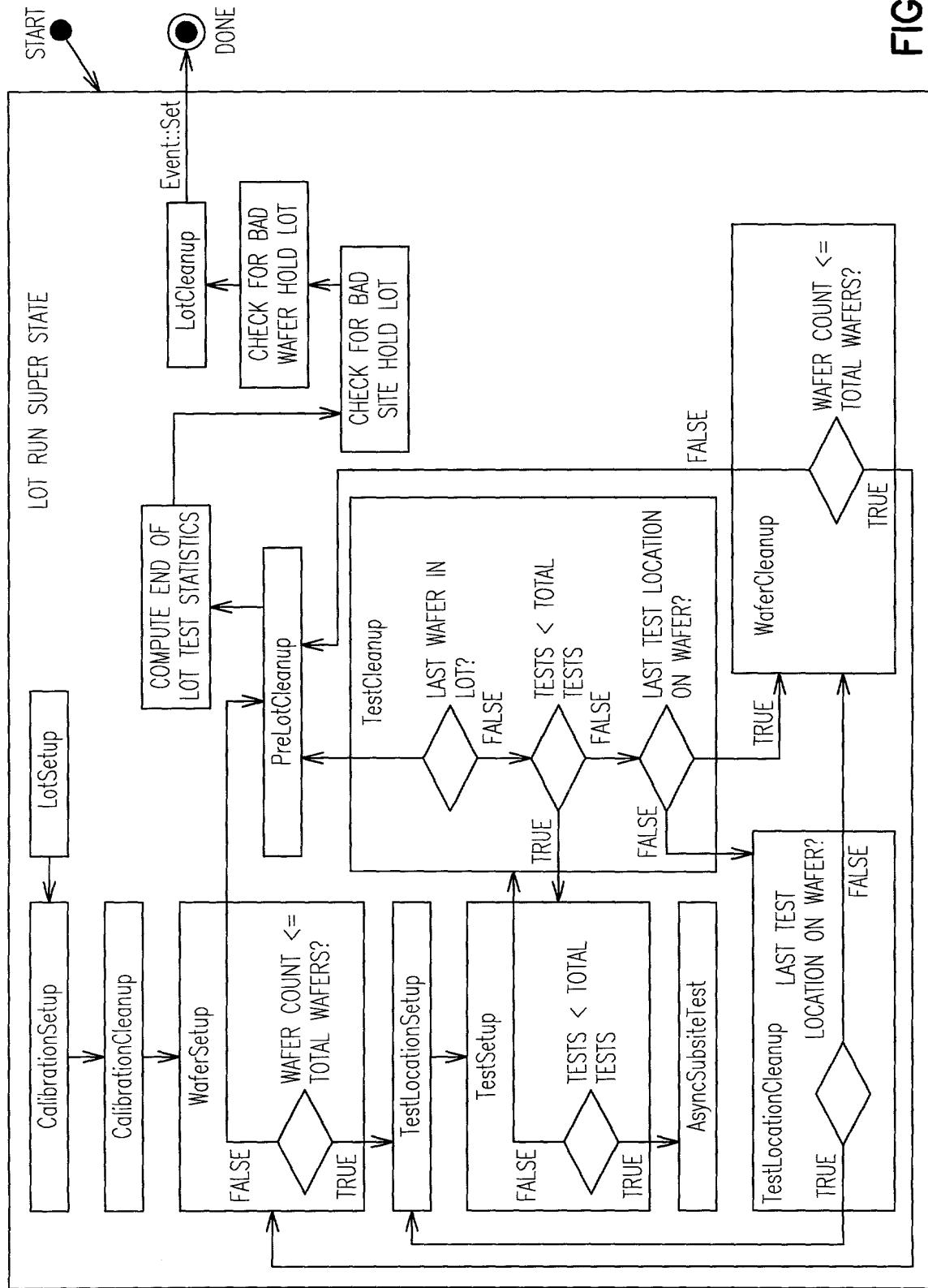


FIG. 6

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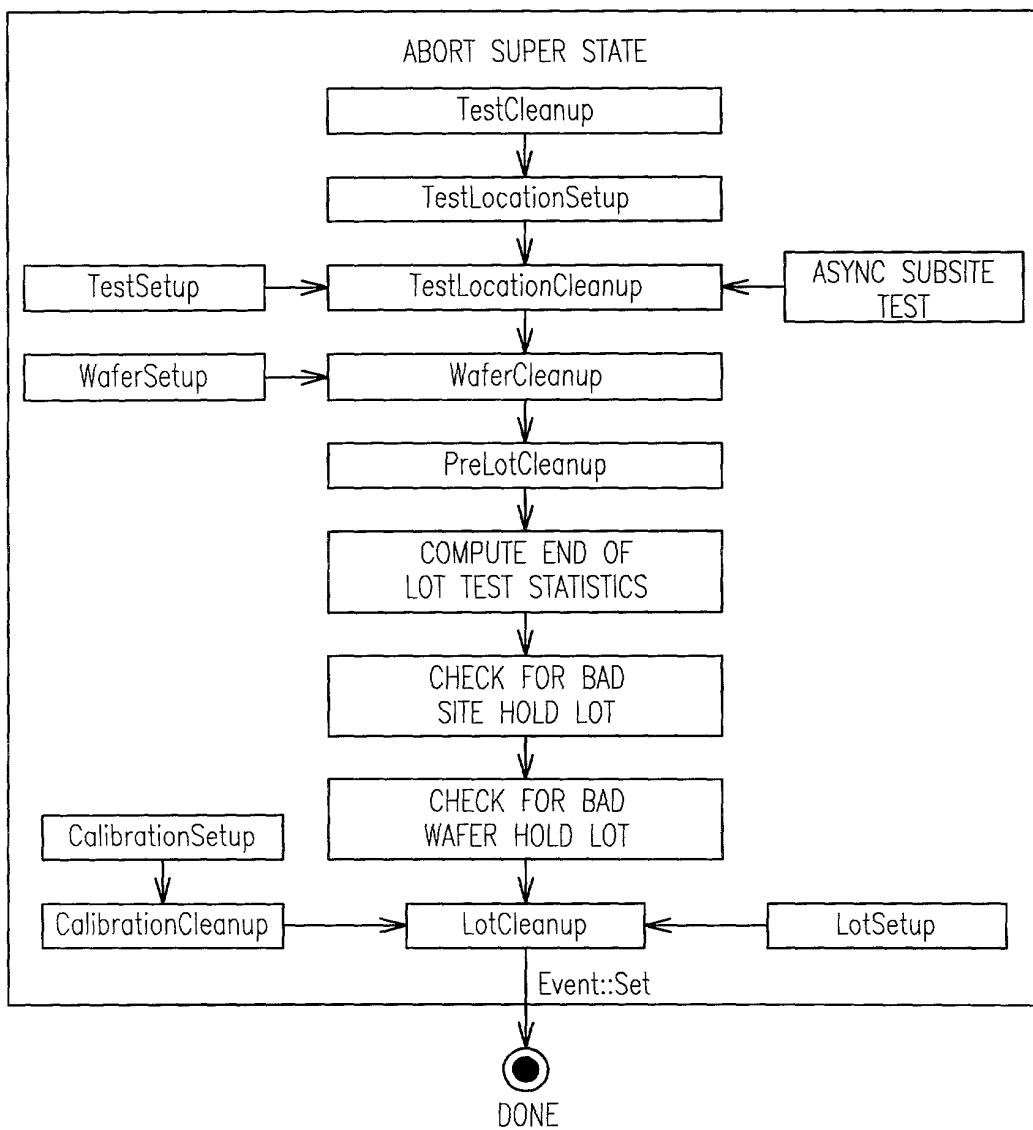
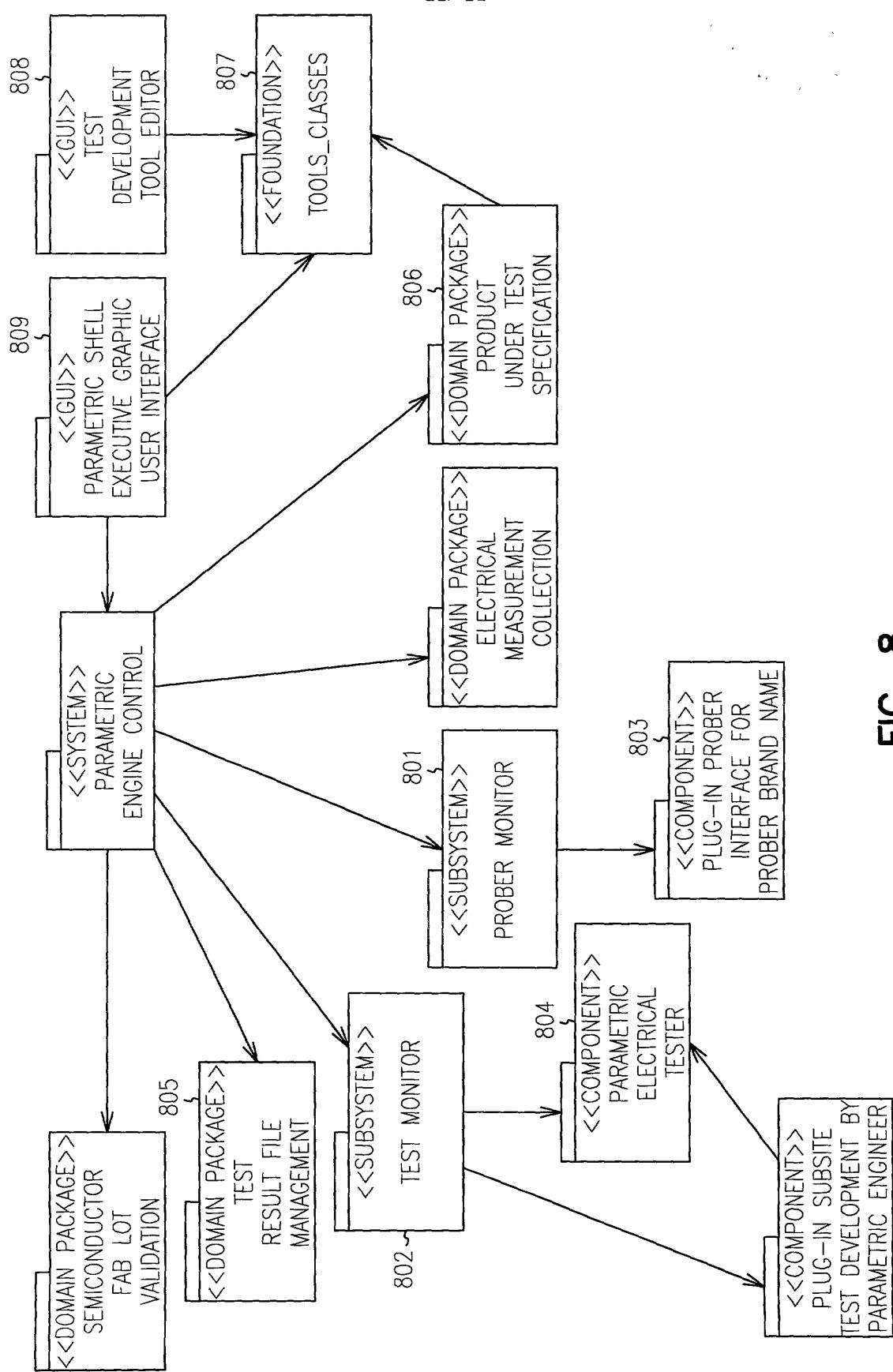


FIG. 7

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**FIG. 8**